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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/900,945	07/10/2001	Toshitada Saito	211200US2	7956
22850	7590	12/08/2003	EXAMINER	
OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C. 1940 DUKE STREET ALEXANDRIA, VA 22314			TRIMMINGS, JOHN P	
			ART UNIT	PAPER NUMBER
			2133	7

DATE MAILED: 12/08/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

09/900,945

Applicant(s)

SAITO, TOSHITADA

Examiner

John P Trimmings

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 10 July 2001.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-12 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-12 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 10 July 2001 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. §§ 119 and 120**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☒ All    b) ☐ Some \*    c) ☐ None of:  
1. ☒ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  
\* See the attached detailed Office action for a list of the certified copies not received.
- 13) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.  
a) ☐ The translation of the foreign language provisional application has been received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 4.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

### **DETAILED ACTION**

Claims 1-12 are presented for examination.

#### ***Priority***

The examiner acknowledges receipt of claim for priority under USC 35 119(a-d) dated 07/10/2001.

#### ***Information Disclosure Statement***

The examiner acknowledges receipt and consideration of applicant's Information Disclosure of 07/10/2001.

#### ***Drawings***

1. The drawings are objected to under 37 CFR 1.83(a) because they fail to show FIG.6, "Internal Control Signal Generator" 15, as described in the specification on page 10 line 35. Any structural detail that is essential for a proper understanding of the disclosed invention should be shown in the drawing. MPEP § 608.02(d). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

#### ***Specification***

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2. The abstract of the disclosure is objected to because the Abstract is longer than 150 words. Correction is required. See MPEP § 608.01(b), 1302.01 ¶ 13.08.
3. The disclosure is objected to because of the following informalities: page 7 recites "control means 30" in line 29, and "selection means 33" in lines 32 and 33. The examiner believes these should read "control means 4", "selection means 30", and "selection means 30" respectively. Appropriate correction is required.
4. The disclosure is objected to because of the following informalities: page 14 line 22 misspells "thinning out". Appropriate correction is required.
5. The disclosure is objected to because of the following informalities: page 15 line 8 recites "particularly been". The examiner believes that it should read, "particularly be". Appropriate correction is required.

### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1, 2, and 10 are rejected under 35 U.S.C. 102(e) as being fully anticipated by Motoki Higashida, U.S. Patent No. 6523136.

As per Claim 1:

Higashida teaches an LSI circuit (column 1 line 20) comprising a storage circuit, peripheral circuits (see FIG. 1), a processor circuit (column 1 lines 5-17) with a program counter, ALU, and register (column 1 lines 18-21 and FIG. 2). There is a selection means for each of the above (column 1 lines 22-37, column 7 lines 15-30, and Fig.'s 2 & 3), as well as selector control by way of a signal via an external terminal (see FIG. 1 9).

As per Claim 2:

Claim 2, being dependent on Claim 1 above, further limits the system to comprise a debug circuit within the MPU that further controls the selector control circuit, and being under control of the processor, as well as the external terminal (column 11, lines 8-54).

As per Claim 10:

Claim 10, dependent on Claim 1 above, further limits the system to having I/O terminal(s) for sending signals to and from a peripheral device. Higashida also explicitly teaches this in FIG. 1 13 and column 5 lines 5-17.

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
  2. Ascertaining the differences between the prior art and the claims at issue.
  3. Resolving the level of ordinary skill in the pertinent art.
  4. Considering objective evidence present in the application indicating obviousness or nonobviousness.
7. Claims 3, 4, 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Motoki Higashida, U.S. Patent No. 6523136, as being obvious.

As per Claim 3:

Claim 3, dependent on Claim 1 above, further limits the system to have three selection units, the 1<sup>st</sup> to select one of the program counter, register, storage, or processor, the 2<sup>nd</sup> to select one of the peripheral circuits, and the 3<sup>rd</sup> to select one of the 1<sup>st</sup> or second. Higashida teaches all of these selectors, the 1<sup>st</sup> in FIG. 2 and column 7 lines 15-30, the 2<sup>nd</sup> in FIG. 3 under control of TP1 and column 7 lines 55-62, and the 3<sup>rd</sup> in FIG. 3 under control of TP2 and column 7 lines 62-67. Instead of the storage being selected in the 1<sup>st</sup> selector as claimed by the applicant, Higashida instead selects the storage units by way of selector 2, and so is not precisely the same as the Claim 3. It would have been obvious to one with ordinary skill in the art at the time of the invention, motivated to use the same bus for storage as for peripherals, to select the Higashida configuration. The examiner does not see any electrical difference in the drawings between the applicant's or the Higashida configuration, and believes that the applicant's configuration may be the same. Being electrically the same, the Claim 3 is rejected.

As per Claim 4:

Claim 4, dependent on Claim 3 above, further limits the system to a debug backup circuit that is controlled by the processor, and controls selection of the 1<sup>st</sup> through 3<sup>rd</sup> selectors as well as the outside signal. Higashida fully teaches this in FIG. 8, by adding the "Register Circuit" 8c in an embodiment of that patent, which derives control from the processor bus (see column 10, lines 54-67 and column 11, lines 1-54), and selects either under control of the processor or external signal.

As per Claim 11:

Claim 11, dependent on Claim 10 above, further limits the I/O terminal(s) to being used for inputting/outputting control and monitor signals. Higashida teaches inputting controls (column 11 lines 1-54) for multiplex controls, outputting monitor signals is not specifically taught. However, the system of Higashida has the same structure as the applicant's, and therefore, under control of the processor, as in column 7 lines 15-67, the same bus which multiplexes monitor data to the monitor output can under the processor control output the data via the I/O bus. One with ordinary skill in the art at the time of the invention, motivated to providing test data without using any more I/O pins as suggested by Higashida in column 4 lines 3-30, would have used only the available I/O pins for test data, or both I/O pins and monitor pins, therefore the Claim 11 is rejected.

As per Claim 12:

Claim 12, dependent on Claim 1, limits the system to one monitor input control signal, and one monitor output terminal during debug. Higashida teaches the input

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control signal (FIG. 1 9), but uses an 8-bit monitor output bus (FIG. 1 12). However, one with ordinary skill in the art at the time of the invention, motivated to providing test data without using any more I/O pins as suggested by Higashida in column 4 lines 3-30, would have used only the available I/O pins for test data, or both I/O pins and one monitor pin, therefore the Claim 12 is rejected.

8. Claims 5-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Motoki Higashida, U.S. Patent No. 6523136 as applied to claims 1 and 3 above, and further in view of Tashiro et al., U.S. Patent No. 5566303.

As per Claims 5 and 6:

Claims 5 and 6 further limit Higashida to multiple processor units on the LSI circuit according to Claim 3, including multiple selection units, control signals, debug units, control circuits, as well as the external monitor control signal. Higashida in the dependent claims above teaches all of this, but does not teach multiple processors. Tashiro et al. does teach multiple processors (see FIG. 11 and 12) in column 1 lines 9-16. One with ordinary skill in the art at the time of the invention, motivated to providing test capabilities to all processors resident on a chip, as suggested by Tashiro et al. (see Abstract), would combine the processors of Tashiro et al. with the system configuration of Higashida, therefore the Claims 5 and 6 are rejected.

As per Claim 7:

Claim 7, dependent on Claim 5, limits the system to a serial to parallel converter for outputting to the outside. Higashida does output an 8-bit signal (see FIG.1 12), and therefore by virtue of the output bus size, does not require a serial/parallel conversion. If

one were required, then as suggested for larger bus widths in column 8 lines 18-29 of Higashida, one would utilize a serial/parallel converter; therefore the Claim 7 is rejected.

As per Claim 8:

Claim 8, dependent on Claim 5, limits the system to a parallel to serial converter for outputting to the outside. Higashida does output an 8-bit signal (see FIG. 12), and would therefore require a parallel/serial conversion. One with ordinary skill in the art at the time of the invention, motivated to providing test data without using any more I/O pins as suggested by Higashida in column 4 lines 3-30, would have used only the available I/O pins for test data, or both I/O pins and one monitor pin, and would require a standard parallel/serial converter. Therefore the Claim 8 is rejected.

As per Claim 9:

Claim 9, dependent on Claim 5 above, further limits the system to use of a thinning-out circuit. Higashida, in column 11 lines 56-67, column 12 lines 1-67, and column 13 lines 1-32, describes the use of flip-flops in-line with monitor data, triggered by a clock. As suggested by column 15, lines 1-6, the examiner recognizes the arrangement of flip-flops to be also a thinning-out circuit, however Higashida does not specify it as such. One with ordinary skill in the art at the time of the invention, motivated to reducing bandwidth of output data would be inclined to change the clock speed of the Higashida invention in order to thin out the signal, therefore the Claim 9 is rejected.

### ***Conclusion***

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to John P Trimmings whose telephone number is 703-305-0714. The examiner can normally be reached on weekdays, 7:30 AM to 4:00 PM.

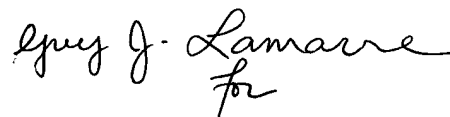
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on 703-305-9595. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-2394.

John P Trimmings  
Examiner  
Art Unit 2133



jpt



Albert DeCady  
Primary Examiner